WEST Search History

DATE: Monday, September 09, 2002

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L24	L23 and l5 and l22	6	L24
L23	l21 adj4 l19	170	L23
L22	l21 adj4 l20	161	L22
L21	prefetch or prefetching	3627	L21
L20	data cache	7021	L20
L19	instruction cache	4176	L19
L18	l17 and (prefetch or prefetching)	1	L18
L17	6199142.pn.	1	L17
L16	l15 and l5	6	L16
L15	L14 and l13	42	L15
L14	(prefetch or prefetching) adj4 (instruction adj (cache or memory))	226	L14
L13	(prefetch or prefetching) adj4 (data adj (cache or memory))	220	L13
L12	l8 and l9	10	L12
L11	l8 and l9 and l5	0	L11
L10	L9 and l8 and l7	0	L10
L9	data prefetch buffer	84	L9
L8	instruction prefetch buffer	121	L8
L7	L5 and (prefetch or prefetching)	93	L7
L6	l5 and l4	1	L6
L5	Harvard architecture	449	L5
L4	L3	76	L4
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L3	(prefetching or prefetch) adj4 l1	98	L3
L2	data adj memory	113340	L2
L1	(instruction or program or code) adj memory	42021	L1

END OF SEARCH HISTORY

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L25	L24 and l18 and l17	153	L25
L24	harvard architecture	449	L24
L23	(memory controller or memory control) same l17 same l18	88	L23
L22	(memory controller or memory control or controller or control unit or control circuit or control circuitry) same l18 same l17	344	L22
L21	memory controller or memory control or controller or control unit or control circuit or control circuitry	468692	L21
L20	L19 same l18 same l17	562	L20
L19	memory controller or memory control or controller or control	1492283	L19
L18	data adj memory	51781	L18
L17	(instruction or code) adj memory	10490	L17
L16	(Rambus or RDRAM) adj interface	50	L16
L15	L14 and l9	20	L15
L14	Rambus.asn.	167	L14
L13	RDRAM.ab.	6	L13
L12	RDRAM.ti.	1	L12
L11	L9 same (l1 or controller or control) same (instruction or code or command) same data	67	L11
L10	L9 same (l1 or controlle or control) same (instruction or code or command) same data	58	L10
L9	RDRAM	426	L9
L8	synchronous dram or SDRAM	3651	L8
L7	L6	220	L7
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L6	L5 and l4	319	L6
L5	l1 same (instruction or code or data) same l3 same memory	428	L5
L4	l1 same (instruction or code or data) same l2 same memory	467	L4
L3	second adj2 bus	12241	L3
L2	first adj2 bus	11991	L2
L1	memory adj2 (controller or control)	102166	L1

END OF SEARCH HISTORY